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# Fuzzy – Discrete wavelet Transform aided SCII based IDVR for Mitigating Power Quality Issues

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***Abstract: This paper emphasize on proposing a fuzzy controller aided switched coupled inductor inverter (SCII) based dynamic voltage restorer for mitigating power quality issues. The system taken here for study comprises of distribution networks having two or more DVR interleaved in each feeder. The traditional DVR topology with a voltage source inverter (VSI) is changed to a switched coupled inductor inverter, which offers an obvious advantage in power transmission over the former. The controller's adaptability is increased in this study by using a fuzzy combine discrete wavelet transform (DWT). The fuzzy and DWT-assisted PWM generation improves the controller's performance by significantly reducing harmonics. The interline dynamic voltage restorer (IDVR) provides a solution for major PQ concerns such as voltage sag and swell, according to simulation and experimental data. In addition, for a load with RL fluctuation, total harmonic distortion (THD) is decreased to 1.46 percent.***

***Keywords: Custom Power devices, Power Quality, Interline Dynamic Voltage Restorer, Switched Coupled Inductor Inverter, Discrete Wavelet Transform, Fuzzy logic***

## 1. INTRODUCTION

The power supply at the load ends is improved by specialized power devices such as the dynamic voltage restorer (DVR), distributed static synchronous compensator (DSTATCOM), and unified power quality conditioner (UPQC). DVR is the most appealing bespoke power device since it compensates for voltage sag/swell, the most common power quality issue. A typical DVR includes an injection transformer with the HV winding linked to the distribution side and the LV winding attached to an inverter, as well as an energy storage device such as a battery, capacitor, or other external sources. On the distribution side, the use of ac drives, welding machines, electronic devices, and other equipment is a major cause of power quality difficulties [1-3]. The compensating power capacity of DVR gets magnified when interline connections are made between DVRs. Interline DVR posses with a common between two DVRs or inverter arrangement. IDVR has proved to be the best in this regard due to its fast energetic response and utilization of energy from external sources like batteries or DC link capacitors and converting it into a single phase or three phase voltages injected in series with the different feeder lines [4-8]. In IDVR, when one of the DVR mitigated voltage sag the other restores DC link energy storage.

The voltage source inverter (VSI) and current source inverter (CSI) are the most common inverter topologies utilised for DVR [9-13]. Two loops will be used in the control technique: a current control loop and a power control loop. The reference voltage for power flow control mode was set using the instantaneous active current acquired from the DC link voltage error signal. The output voltage reduction and enhancement in VSI / CSI are facilitated either by the front end buck-boost converter or back-end transformer. In contrast, the switched coupled inductor inverter (SCII) possesses inherent buck-boost operation within the inverter itself. At the outset, it may be related to a Z source inverter (ZSI), but the former is advantageous since it has only half the number of passive components used in ZSI. The voltage gain of SCII is also high compared to ZSI. Shoot through state and non-shoot through state are the two modes of operation for SCII. [14].

The Wavelet Transform (WT) is a useful tool for identifying and analyzing distorted source waveforms, which is necessary for proper compensation. This technique decomposes the signal at different frequencies that occur in power system transients. After decomposition of the signal, low pass filter and high pass filters are designed to extract the signal from a specified bandwidth. The wavelet transform is used to suppress harmonic distortion in the power system [15-25]. By doing so, it identifies and rapidly rectifies poor power quality signal such as voltage sag, swells, interruption, switching transients and harmonics. The typical PWM way of control possesses sluggish response which affects the appropriate time of inter-line dynamic voltage restorer (IDVR) intervention adversely and therefore a fast and reliable PWM generation is always in demand. Fuzzy logic controller (FLC), a well-entrenched control scheme is fast and very reliable. The fuzzy controller is intelligent in processing the raw data and turns it into useful information.

Overall, this article is unique in that it presents SCII-based IDVR for PQ mitigation, which has never been done before by other scholars. The SCII used in this study has a distinct advantage over the traditional ZSI. The ZSI features a higher number of passive components, which slows the reaction and adds to the cost.

The course of paper is organized as follows: section 2 deals with the system configuration of the work and control strategies of the IDVR. The simulation and hardware results are dealt with in section 3. The comparative analysis of the proposed and existing work has been presented in section 4. Section 5 renders the conclusive remarks of the work

## 2. SYSTEM DESCRIPTION:

IDVR consists of two or more DVR's connected with a common DC link. Each DVR consisted of an inverter with an injection transformer, filter and connected the common DC link capacitor. The DWT as a filter is used for eliminating the excessive harmonic content present at the output of the inverter. Figure 1 presents a schematic diagram of an IDVR with SCII where the two DVRs are connected across a common DC link. Here a control strategy of the Fuzzy logic controller with DWT as a filter is used for triggering the switches in the inverter. The displacement angle or phase advance angle of the voltage input during a fault is taken into consideration for giving the reference input voltage.

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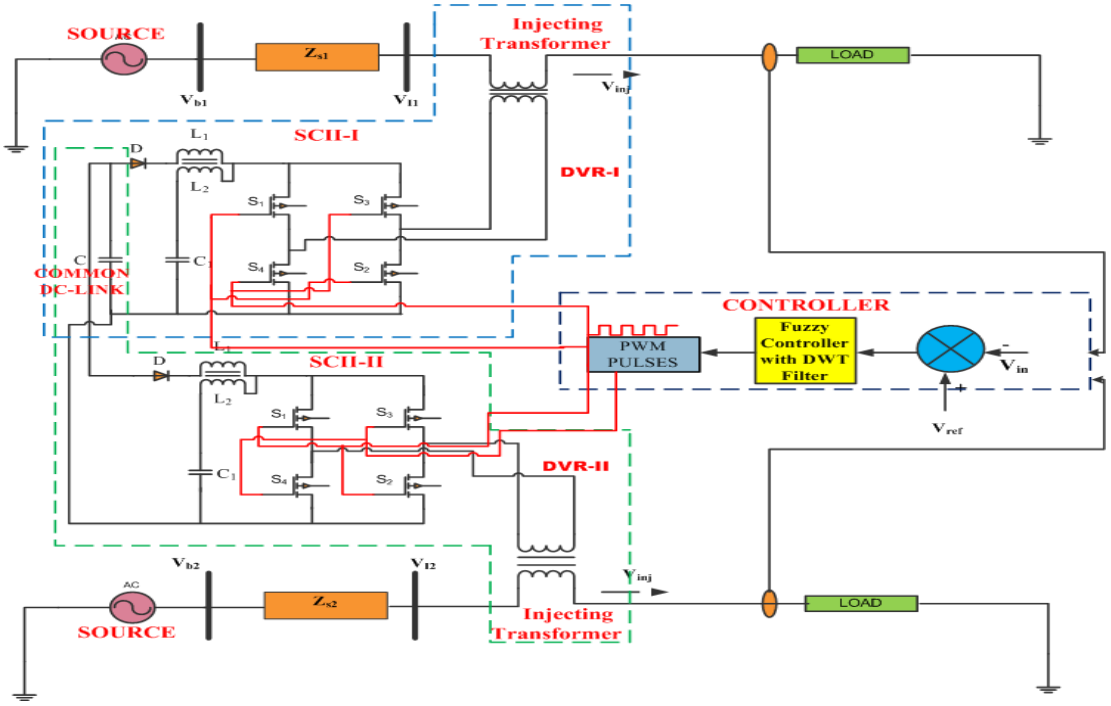
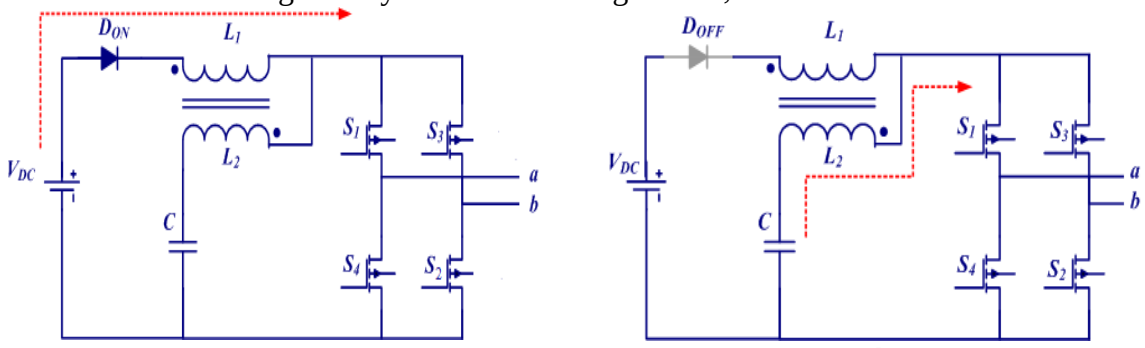



Figure 1. Schematic diagram of Inter-line Dynamic Voltage Restorer

When a failure occurs on either of the feeders, power is sent between two DVRs via a DC link capacitor. To mitigate the situation, the defective feeder's DVR functions in a compensatory mode. The reference voltage across the DC link capacitor and the load voltage with its phase angle were used in the control circuitry for triggering the switches in the inverters.

### 2.1. *The operational control strategy of Switched Coupled Inductor Inverter:*

Because of its high voltage buck-boost capacity, SCII has replaced traditional VSIs/CSIs, as seen in Figure 2 (a) and (b) (b). It works on the same idea as a Z source inverter (ZSI), but uses half as many passive components and has a higher shoot through capability for the same voltage gain [14]. The switches in the same leg are switched on at the same time during shoot through to facilitate a short and create a voltage in the inductor. In non-shoot through mode, the inverting operation is performed. Due to the inclusion of a diode in a normal ZSI, there is a risk of switches being destroyed in shoot through mode, but this is not the case in a SCII.



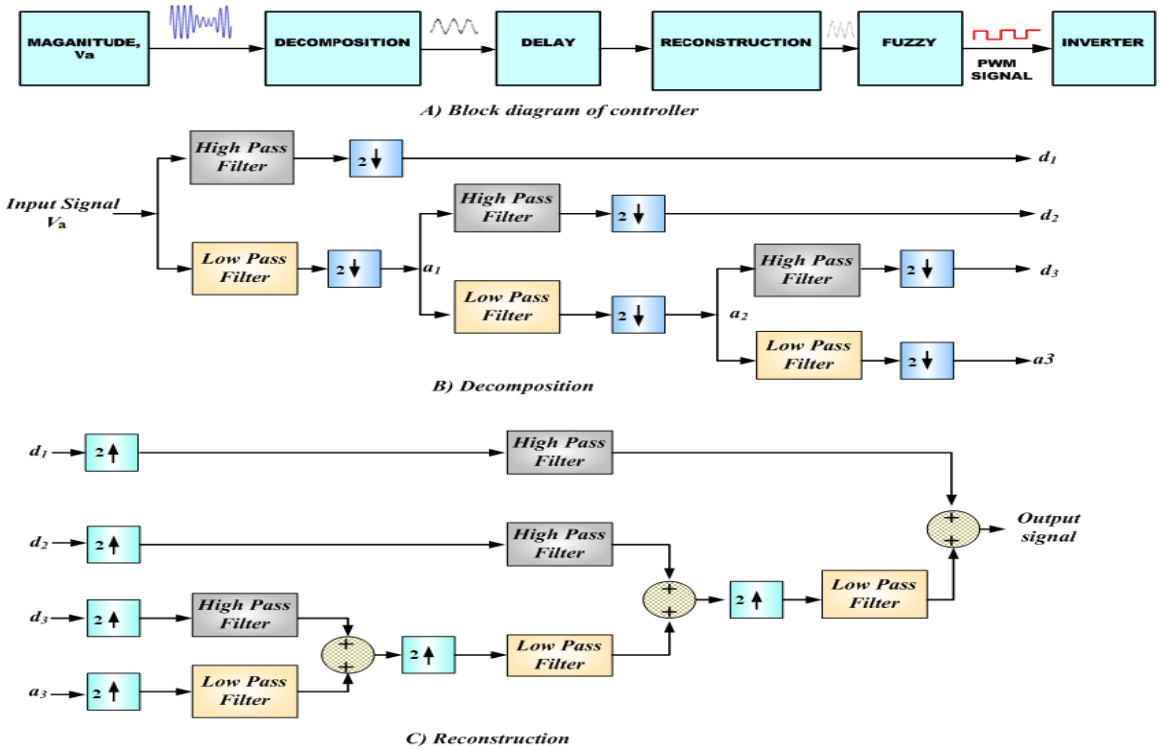

(a) (b)

Figure 2 (a) SCII during a normal state, (b) SCII during shoot through the state

Under typical circumstances, current flows from the source to the connected inductors and then back through the inverter's MOSFETs. During this time, the inductor winding L2

has charged the capacitor C. The capacitor discharges via the switches during the shoot through period, as does the inductor L2.

### 2.3. Controller strategy of Discrete Wavelet Transform:




The DWT technique of digital filtering is used to decompose the signal into distinct levels. DWT stands out from the crowd when it comes to signal processing techniques for stationary and non-stationary signals. It generates a Multi-Resolution Analysis (MRA) that is similar to a bank of filters with a constant relative bandwidth. The filter bank is used by DWT to create time-frequency analyses. As demonstrated in Fig. 4, a discrete signal can be filtered at three levels using the analysis bank and synthesis bank methods. The frequency content of the incoming signal is separated using DWT. As shown in Figure 4, an input signal of load voltage Vab is communicated as a vector utilizing a buffer provided to the DWT system (A). A DWT is used to separate the decomposing and reconstruction signal using the Multi-Resolution process as shown in Figure 4 (B) and (C). DWT co-efficient are $d_1$, $d_2$, $d_3$, $a_1$, $a_2$, and $a_3$ as shown in Figure 4 (B and C). The computation as obtained by the following equations given below (1)-(6) of the coefficient. The output of the filter for each signal contains half of the frequency content. The sampling frequency contains an input signal for the low and high pass filter; this structure is called DWT [18]. Therefore downsampling and an upsampling factor of two, denoted by2 ↑and 2↓ respectively as applied to the output of the filter in the analysis and synthesis bank. This signal is given to the fuzzy logic controller.

Figure 4. Schematic diagram of DWT

$$d_1 = \sum_{n=0}^{L-1} h(n)x(2K-n) \quad (1)$$

$$d_2 = \sum_{n=0}^{L-1} h(n)xi1(4K-2n) \quad (2)$$

$$d_3 = \sum_{n=0}^{L-1} h(n)xi2(8K-4n) \quad (23$$

$$a_1 = \sum_{n=0}^{L-1} g(n)x(2K-n) \quad (4)$$

$$a_2 = \sum_{n=0}^{L-1} g(n)xi2(4K-2n) \quad (5)$$

$$a_3 = \sum_{n=0}^{L-1} g(n)xi2(8K-4n) \quad (6)$$

Where L is filtered length

### *2.4. Fuzzy Logic Controlled Strategy:*

The discrete voltages are taken and are subtracted from their respective reference voltages generated considering the load advance angles, this gives the error signal for each component. The change in error signal has obtained by differentiating the error signal. FLC is known for being a dynamic and intelligent tool for solving the non-linear problem. Similar to the conventional controller, FLC does not need a mathematical model for the system. Understanding of the complete system its control requirement is comparative for framing the rule base. The design of the FLC is made using the information/data flow as input. It has followed by getting processed with a decision-making engine, and its corresponding control signal has obtained along with the defuzzification engine. Figure 5 shows the three stages.

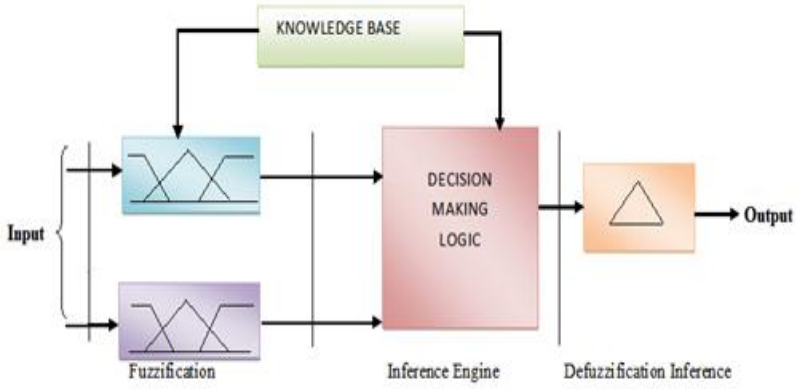



Figure 5. Structure of Fuzzy controller stages

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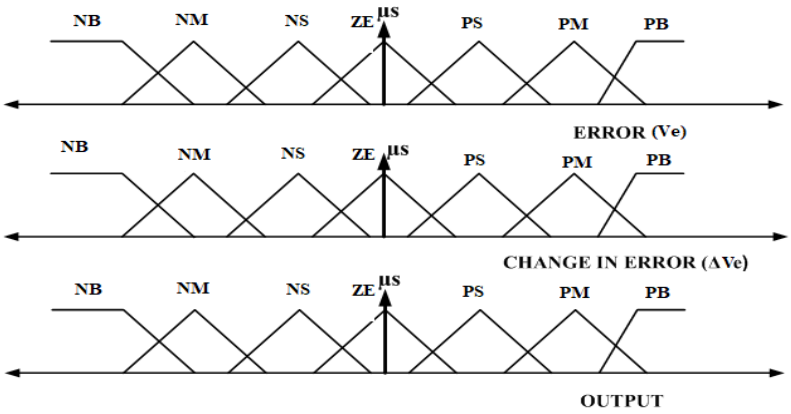


Fig. 6. Membership functions

The error voltage (Ve) and its derivative (Ve) have been multiplexed. Details are fed into the FLC as input. The control signal for FLC is then sent to the logic circuits, allowing for the generation of high-frequency pulses. The switches Q1 and Q2 receive the frequency variable pulses, which are used to track the voltage set. Figure 6 depicts the input to FLC, which is separated into seven membership functions and labelled as tabulated. Fuzzy control rules have been constructed using fundamental control knowledge without taking into account the plant's mathematical model. The fuzzy rule basis is shown in Table I. The rule base contains simple language rules that aid in the execution of the control action.

Table I: Rule base for the fuzzy logic controller.

| the $V_e/\Delta V_e$ | NB | NM | NS | ZE | PS | PM | PB |
|---|---|---|---|---|---|---|---|
| NB | NB | NB | NB | NB | NM | NS | ZE |
| NM | NB | NB | NB | NM | NS | ZE | PS |
| NS | NB | NB | NM | NS | ZE | PS | PM |
| ZE | NB | NM | NS | ZE | PS | PM | PB |
| PS | NM | NS | ZE | PS | PM | PB | PB |
| PM | NS | ZE | PS | PM | PB | PB | PB |
| PB | ZE | PS | PM | PB | PB | PB | PB |

## 3. RESULTS AND DISCUSSION:

### *3.1. Simulation:*

Simulation for a single phase IDVR between two feeders each consisting of 50V in MATLAB-Simulink has been carried out. The corresponding DVR is connected between the source bus and the load bus. The DC link capacitor value is chosen as 250μF. The fault conditions are simulated, and the output results are shown in this section. Initially, in feeder 1 a fault occurs and due to this voltage sag is formed as shown in Figure 7 (a). The compensation voltage to be injected in the feeder 1 is shown in Figure 7(b). Figure 7 illustrates the cumulative compensated voltage (c). SCII, in conjunction with the control loop, performs a compensation action to restore the voltage that was lost due to sag. When an

unload period occurs in feeder 2, a voltage surge occurs, which must be decreased.: An input signal to the DWT structure will be a load voltage of magnitude, Van, and phase. DWT's digital filtering will split the signal into several levels, such as coefficient of d1, d2, d3, and a3. This signal reconstructs the module by combining as a low pass and high pass filter with sampling factors of 2 and 2 respectively. The combination of detailed and approximation coefficients is used to rebuild the original signal. The synthesis output signal is fed into the fuzzy controller as an input. For framing the rule basis, it was discovered that understanding the entire system, including its control requirements, was required. The information/data flow has been used to design the FLC. It was then processed with a decision-making engine, and the de-fuzzification engine was used to obtain the relevant control signal. The desired output is taught by generating a PWM signal and feeding it to the inverter's gate pulses. This voltage was injected by SCII through a transformer near the load. As a result, harmonics are eliminated, and voltage sag, voltage swell, and interruption are reduced. During a voltage sag, it compensates for 50% of the voltage.

During load variation, a voltage sag of 25V magnitude occurred with a time ranging from 0.1 to 0.3 seconds, and a ground impedance value of 0.85 is considered in feeder1. The peak voltage from the source voltage is decreased to a nominal value of 50V to 25V under steady-state operation conditions. The inverter's common DC link capacitor voltage eliminates voltage sag and restores the constant state. The output voltage without, injecting inverter voltage and with compensation is shown in Figure 7 (a), Figure 7 (b) and Figure 7 (c )respectively. DC link voltage of 32V as required for constant voltage during fault condition as shown in Figure 7 (d).

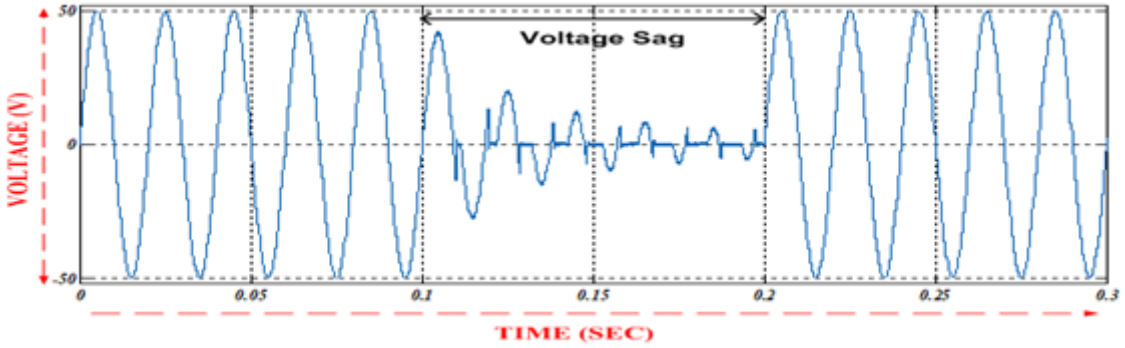


Figure 7 (a). Voltage Sag _without compensation_Feeder1

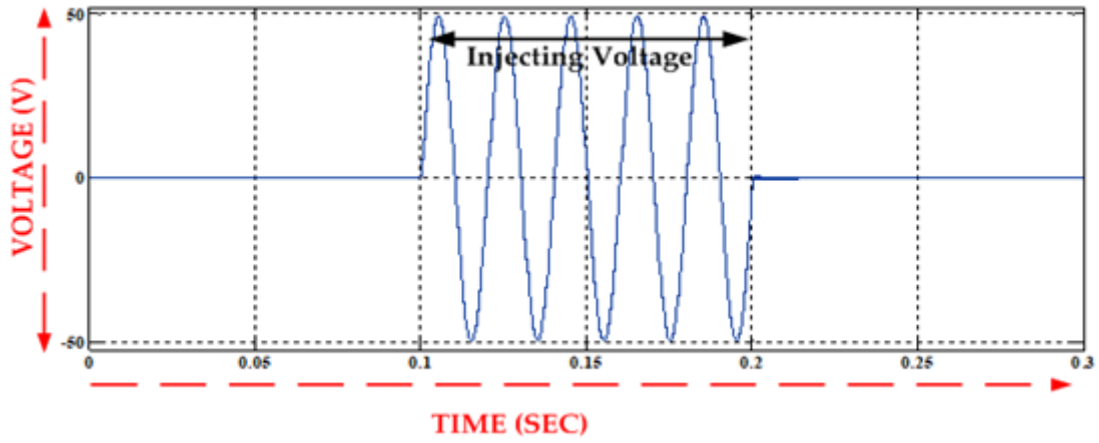


Figure 7(b). Voltage Sag_Injecting Inverter_Feeder 1

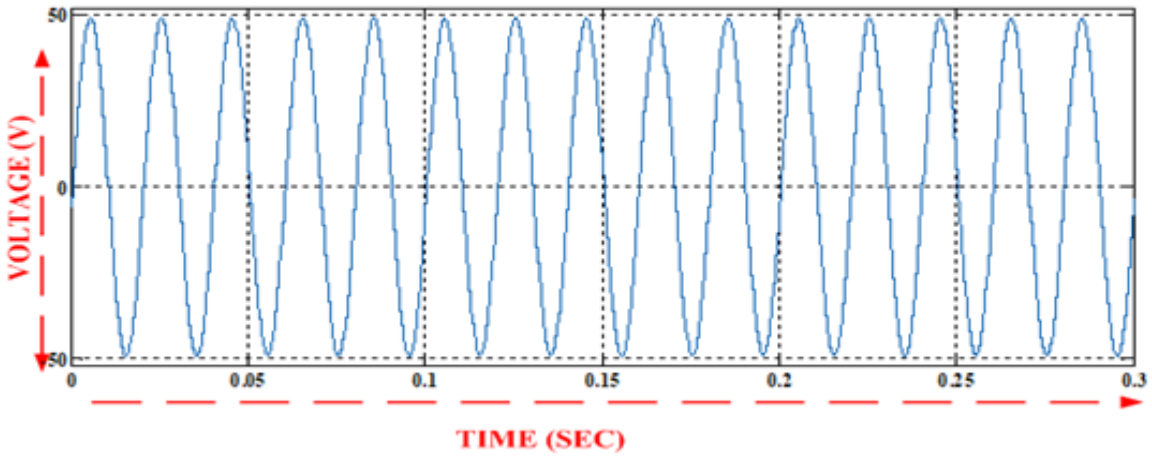


Figure 7(c). Voltage Sag _with compensation_Feeder1

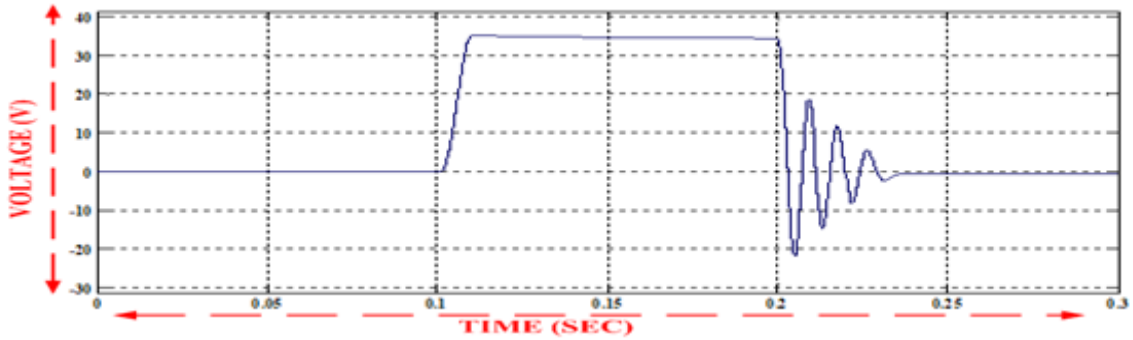


Figure 7(d). DC Line Voltages

Fault and ground impedance value of 0.01 as considered in feeder 2 caused a momentary interruption of 48V magnitude and duration ranging from 0.3 to 0.4 seconds. The peak voltage from the source voltage was decreased from 50V to 2V during steady-state working circumstances. A balanced supply as needed for the load, as well as a common DC link capacitor voltage through the inverter, removed the voltage interruption and returned the system to a steady condition. Figures 7(e) and 7(f) illustrate the output voltage without and with correction, respectively.

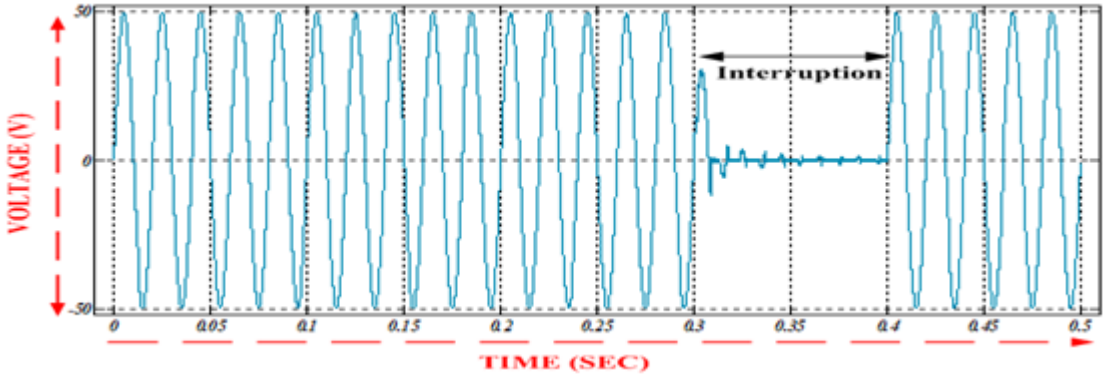


Figure 7(e). Voltage Interruption _Without Compensation_Feeder 2

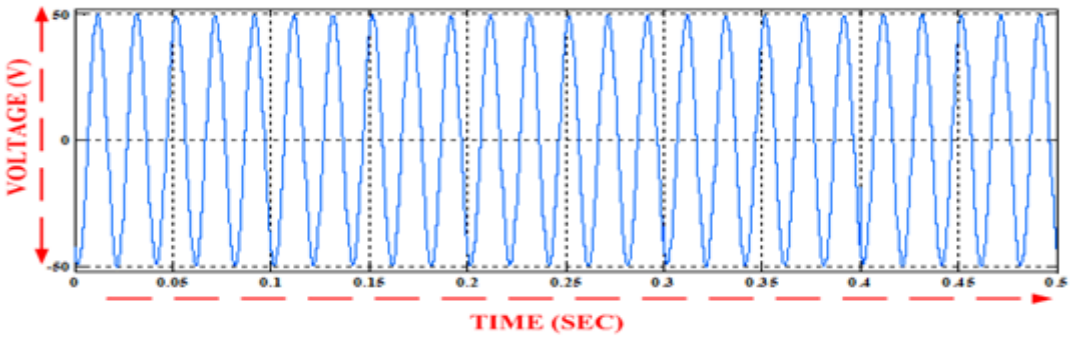


Figure 7(f). Voltage Interruption _With Compensation_Feeder 2

When there is the sudden exclusion of load, or an additional capacitance has been added in feeder 1, as a consequence, there is a voltage swell of 10V magnitude with duration ranging from 0.25 sec to 0.35 sec occurs. The peak value of the source voltage rises from a nominal value of 50V to 60V during steady state operating conditions. A common DC link capacitor voltage through the inverter reduced the voltage swell and returned the voltage to its steady condition, as needed by the supply voltage to the load.The output voltage without and with compensation are shown in Figure 7(g) and Figure 7(h) respectively. The output current was carried out 0.8A as shown in Figure 7(i).

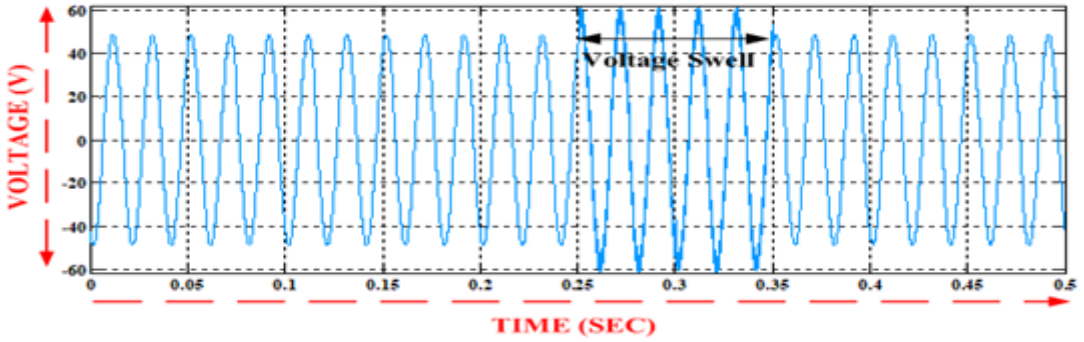


Figure 7(g). Voltage Swell_Without Compensation_Feeder 2

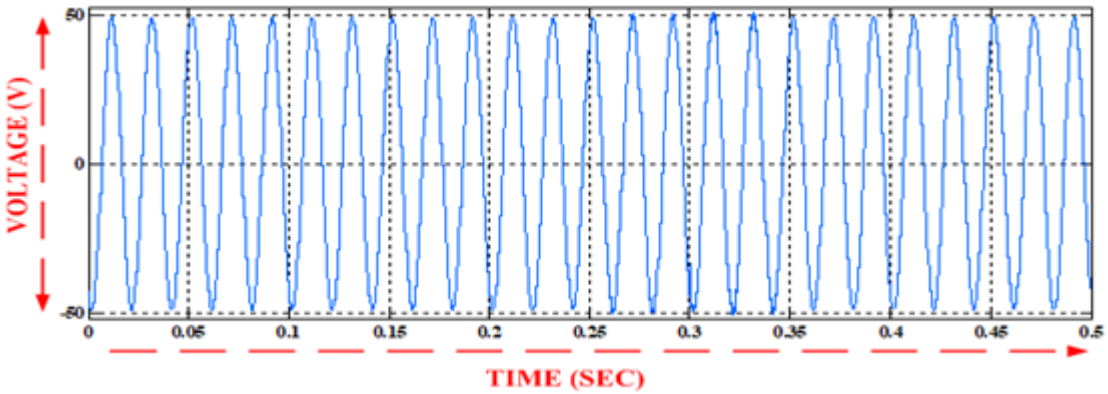


Figure 7(h). Voltage Swell_With Compensation_Feeder 2

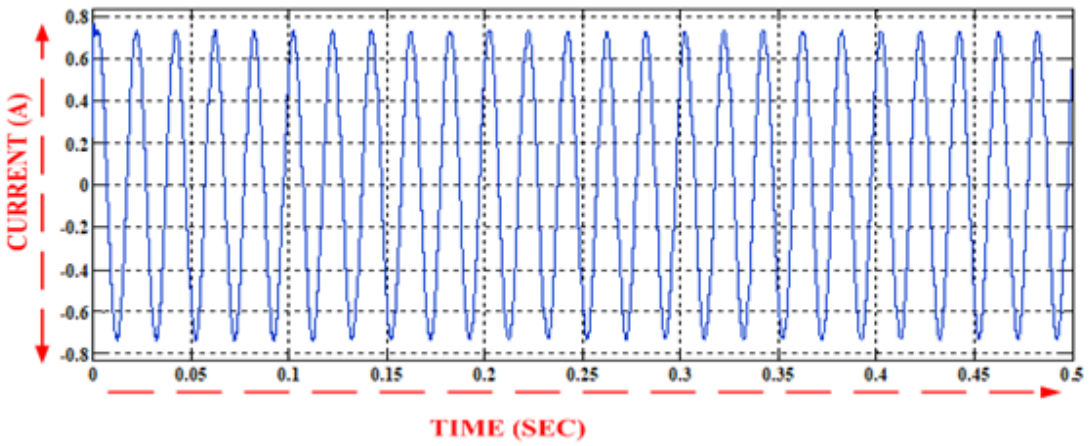


Figure 7(i). Current _Feeder 2

FFT analysis has been carried out to analyse the presence of harmonic content in the output for the output voltage for determining the percentage of harmonics present. Figure 8(a) to Figure 8(e) shows the reduction in the current to THD value of less than 5% within the IEEE standard. The harmonics are reduced due to a smaller number of passive components used in the inverter circuits. The ability of IDVR aided SCII in protecting the distribution system from variation in loads occurring in either of the feeders (Feeder1 and Feeder2). The common DC link voltage Vdc has also been found to work satisfactorily. Figures 8(a) and 8(d) demonstrate that the Total Harmonic Distortion (THD) before adjustment at the load side for voltage sag and swell is 34.52 percent and 6.32 percent, respectively. THD after compensation for voltage sag and swell at the load side is 0.14 percent and 0.10 percent, respectively, as shown in Figures 8(b) and 8(e).

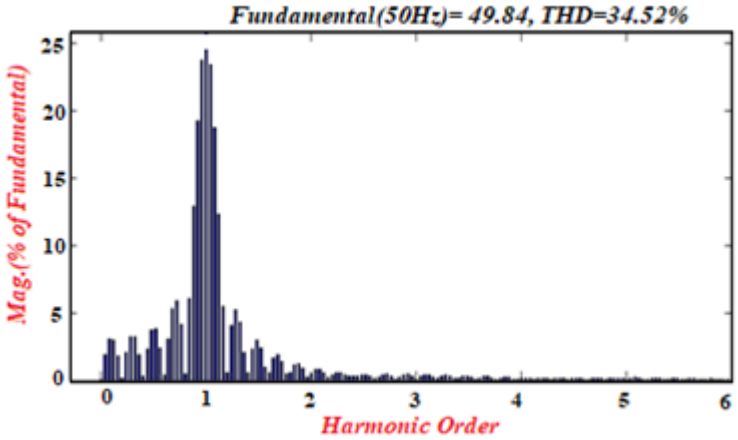


Figure 8(a). FFT Analysis of Harmonics Content under voltage sag

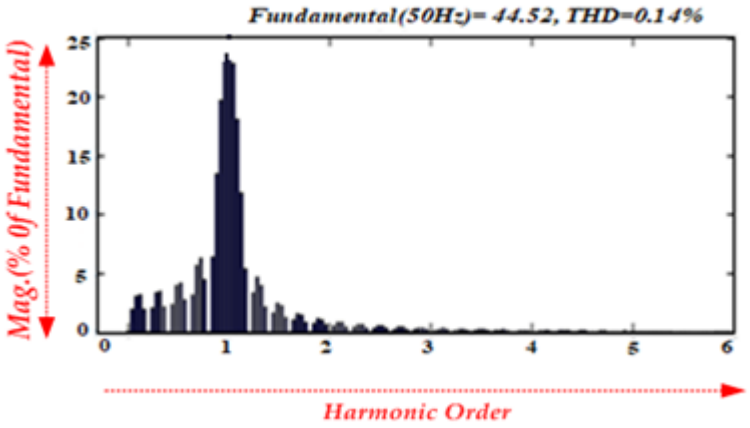


Figure 8(b.) FFT Analysis of Harmonics Content _voltage sag compensation

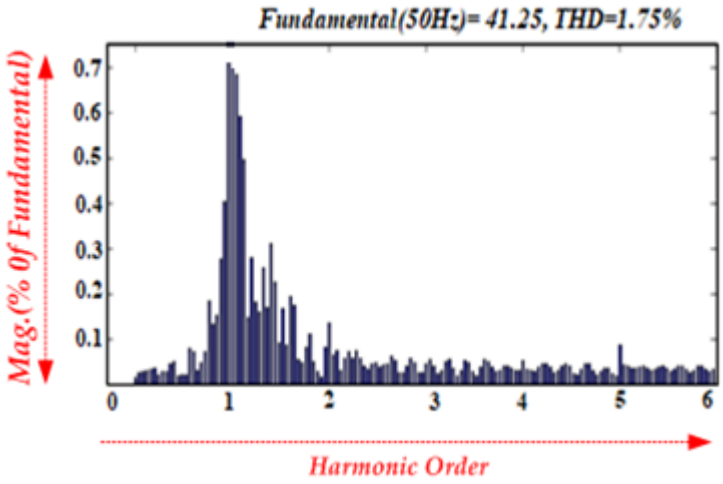


Figure 8(c). FFT Analysis of Harmonics Content_ during voltage interruption compensation

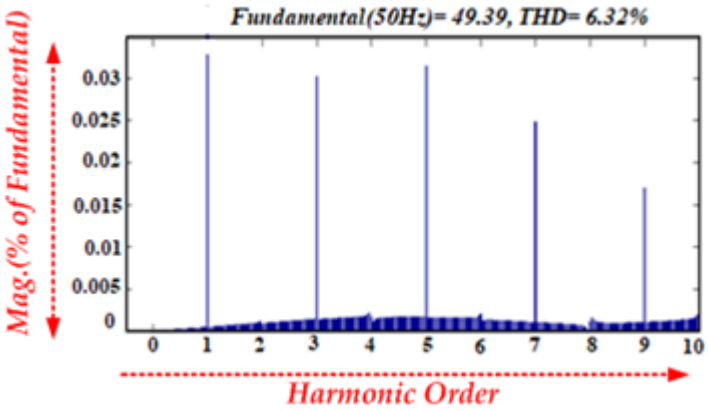


Figure 8(d). FFT Analysis of Harmonics content under Voltage Swell

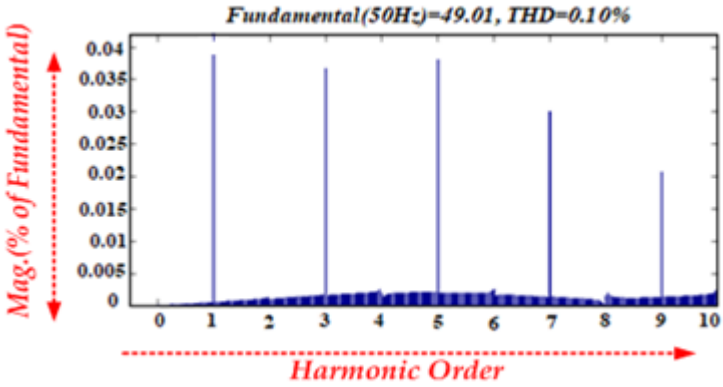


Figure 8(e). FFT Analysis of Harmonics Content during Voltage swell compensation

## 4. CONCLUSION:

This paper proposes a single-phase IDVR as a PQ issue mitigation device. In the distribution side, the IDVR with SCII mitigates power quality issues such as voltage sag/swell, interruption, and harmonics. The load variation is the constraint aspect of the IDVR system in terms of power exchange between the feeders. When one of the DVRs is utilised to mitigate voltage sag/swell, the energy is replenished utilising DC-link stored with maintaining a constant voltage by the other DVRs. When a result, the THD value drops to 0.14 percent and 1.46 percent of harmonic content as the fault state changes. According to the findings, the IDVR system can compensate for 50% of PQ difficulties such as voltage sag/swell over a long time.

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