International Journal of Aquatic Science
ISSN: 2008-8019
Vol 12, Issue 03, 2021

Implementation Of A Simplified Nine Level Dc-Ac Inverter

Satish Kumar S[1], Dr M. Sasikumar[2], Dr P Sivaperumal[3], JS Ashwin[4], Kavitha Kumari K S[5]

[1,3,4]Assisant Professor, Academy of Maritime Education and Training, Chennai-603112,India
[2]Professor, Jeppiaar Engineering College, Chennai – 600 119, India
[5]Assistant Professor, Arupadai Veedu Institute of Technology,Chennai-603104,India

Email: [1]satishkumar.s@ametuniv.ac.in, [2]pmsasi77@gmail.com., sivaperumal@ametuniv.ac.in[3] and [5]kavithakseee@gmail.com

Abstract: In recent years, cascaded Hi-Bridge multilevel inverter is preferred many of ithe industrial applications. Cascaded H-bridge iMultilevel Inverter know-hows became an incredibly is the important optimal medium voltage and high power control. In the conventional system, seven levels AC output voltage is obtained by using eight switches with appropriate gate signal design. The conventional system is controlled by the iSinusoidal Pulse Width Modulation (SPWM) technique. The projected imultilevel inverter produces Nine level alternating current output voltage with reduced number of switches. The control technique used here is iSinusoidal Pulse Width Modulation (SPWM) technique by TMS320LF2407i digital signal processor (DSP). The main advantage of this technique is reduced harmonic distortion, reduced number of switching power devices and decreased switchingi losses. The projected system voltage stress are reduced. The conventional multilevel inverter (MLI) and proposed Modified Cascaded Hi Bridge Multi Level Inverter (MCHBMLI) are simulated to compare their Total Harmonic Distortion. To conclude, a iLaboratory prototype multilevel iinverter has output voltage of 220v/2 KW with 400v input voltage is realized. Investigational results display the efficacy at full load is 94.6% and the efficacy at the maximum s 96.9%.

Index Terms—i Multi-Level iInverter (MLI), Modified cascaded Hi Bridge Multilevel inverter (HCBMLIi), is Sinusoidal iPulse Width Modulation (SPWM) Total harmonic Distortion (THD)

1. OVERVIEW

Nowadays iMultilevel iInverters are generally used in iindustrial uses. And they are used in the zones where we essential high power required. The ikey purpose of inverter is the iswitching frequency. To alter Direct Current signal into a Alternating Currenti signal, we need a firm switching of Direct Current signal giving us multiple levels. This turns into a set of steps wave that is quite close to a sine wave. {1-8} Thei difference between a humble inverter and a Multilevel Inverter is as follows,

- Multileveli inverters stretch higher power.
-They are functioned through Multiple switches iinstead of onemany

This itopology was first anticipated in 1981.They are also called as Neutral Point Inverters. In 1992, a lot of investigation works was issued on Diode Clamped Multilevel iinverters. They have their fair share of merits and demerits tied to them.

The use of capacitors and diodes for transposal. The purpose is to adapt the Direct Current voltage into a capacitor voltage. Proper iprecautionary actions are taken in order to avoid over charging of capacitors. Here we utilize diodes to maximum the influence devices voltage istress {9-15}. The potentialacrross the each devices is Vdc. The switching angle should be considered in such a way that the THD of output voltage should be as low as conceivable. In his method lowerest overriding harmonics can be eliminated by taking designed switching angles. Simply, they convert dc voltage into capacitor voltage. As name suggests they need clamping devices such as diodes.

Flyingi Capacitori Multilevel Inverter

This a pretty well-known topology and it is similar to Diodei Clampedi iMultilevel Inverter the input voltages are divides equally using the capacitor {16-20}. One of the key rewards of using Flying Capacitor iinverter is its aptitude to function at voltages advanced than the obstructive capacity of each cell involving of diode and switching elements. It is also called as imbricate cell multilevel inverter.

CONSERVATIVE HYBRID CASCADED FIVE LEVEL INVERTER

As a consequence growth of our technology, the electrical power demand is more than. the progression of semiconductors, the promotion of power electronics devices specification of improvement of power. Therefore, the harmonic pollution of power system regulations and standards have been formulated to harmonics are controlled and electrics equipment controlled power factor. Furthermore, the industry ultimatum higher power applications, the description of power device is higher. MOSFET in this section the function at high frequency. To obtaining the reduced harmonics in multi-level inverter, various topology are utilize to minimum rating constituent at high power application. The resolution of multilevel topology is to decrease voltage rating of power switch. By adding the output voltages in multilevel form, it has advantages of low dv/dt, low iinput current distortion, and lesser switching frequency. The novel iMultilevel Inverter is intended and applied in this paper. The major feature of the proposed topology is the reduction of power components. The Sinusoidal Pulse-Width iModulation (SPWM) is used to control existing circuit by TMS320LF2407 Digital Signal Processori (DSP)..

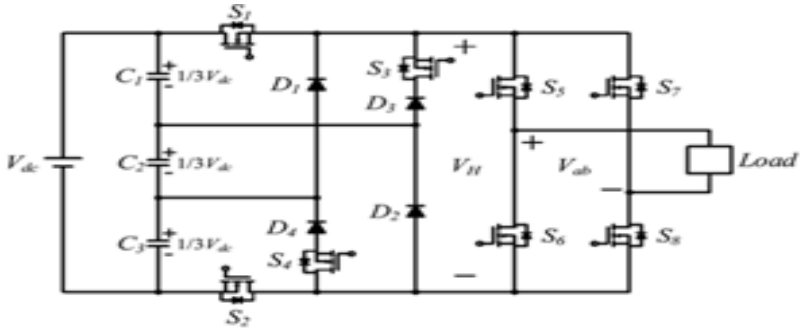

Figure 2.1: The conventional seven level topology

Fig. 2.1 shows the novel topology used in the Seven Level iInverter. An input voltage barrier is collected of three series capacitors C1, C2, and C3. The separated voltage is transmitted to Hi-bridge by four MOSFET, and four diodes. The voltage is send to output terminal by H-bridge which is formed by four MOSFET. The proposed iMultilevel Inverter generates seven levels Alternating Current output voltage with the suitable gate signals strategy.

International Journal of Aquatic Science
ISSN: 2008-8019
Vol 12, Issue 03, 2021

SUGGESTED HYBRID CASCADED NINE LEVEL INVERTER

The proposed system generates s level output with appropriate gate signal design. This system reduces the switching ilosses and harmonic distortion with the reduced number of switches. Here, eight switches are used to generate Nine level Alternating Current output voltage.

No. of switches = (N+5)/2

No. of voltage sources, V = (N-1)/2

The required Nine voltage output levels (±5V,±4V,±3V,±2V,±V,0) are generated as follows:

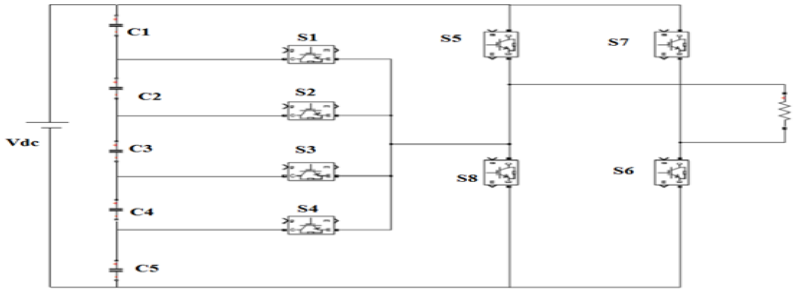

Figure 3.1: Suggested HCMLI

Fig 3.1 shows the novel customised topology used in the Nine level inverter. The Input Voltage separator is composed of five series capacitors *C*1, *C*2,C3,C4 and *C*5. The separated voltage is communicated to H-bridge by four IGBT. The output voltage observed across the switches. The projected Multilevel Inverter makes Nine levels Alternating Current output voltage with the appropriate gate signals design.

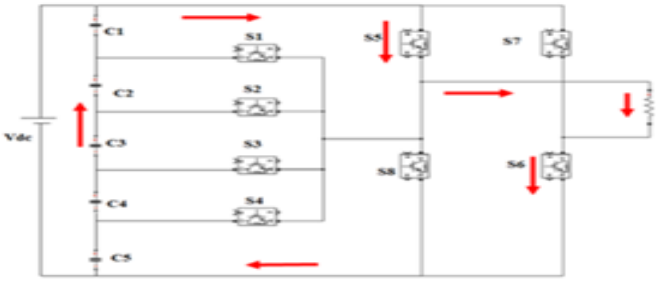

Figure 3.2(a) Mode 1

To produce a voltage level V_0 = 5V, *S*5 and S6 is turned ON at the positive half cycle. Vitality is providing by the capacitor *C*1, C2,C3,C4 and C5.The voltage across load is 5V. Fig..3.2.(a) displays the.

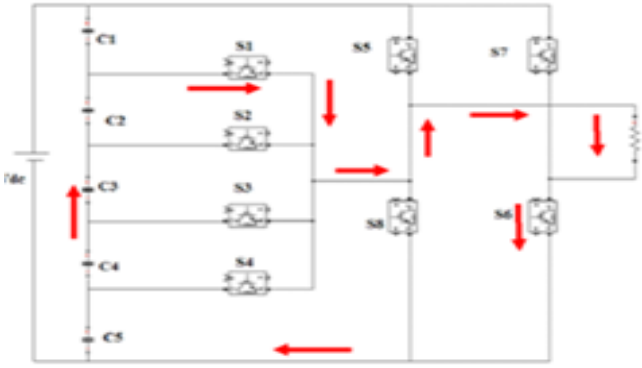

Figure 3.2(b) Mode 2

To produce a voltage level V0 = 4V, S1 and S6 are turned ON. Vitality is providing by the capacitor C2,C3,C4 and C5.The voltage across load is 4V. Fig.3.2.(b) displays the current path at this e.v

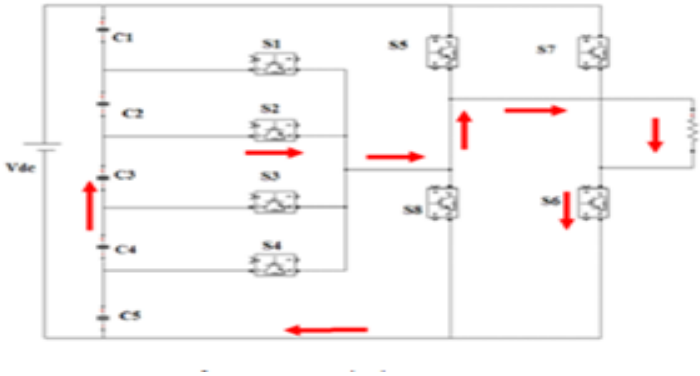

Figure 3.2(c) Mode 3

To produce a voltage level V_0= 3V, *S*2 and *S*6 are turned ON. Dynamism is providing by the capacitor *C*3,C4 and *C*5.The voltage across load is 3V. Fig..3.2.(c displays the current path at this mode.

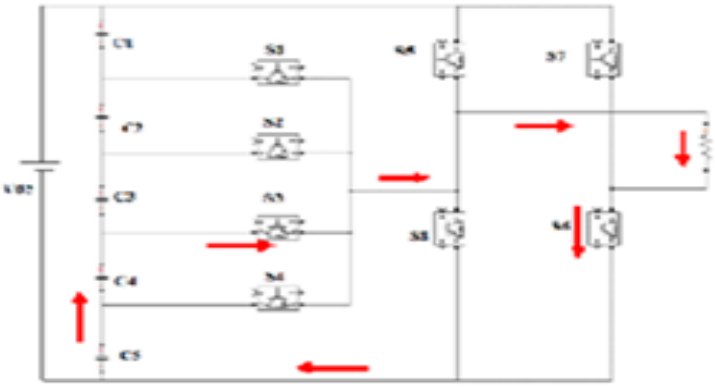

Figure 3.2(d) Mode 4

ON at the Negative Half cycle. Energy is providing by the capacitor C1,C2,C3,C4 and C5.Thevoltage across the load is -5V.Fig.3.2.(k) displays the current path at this mode.

Table 3.1Switching table

c	1	2	3	4	5	6	7	8
4V	1	0	0	0	0	1	0	0
3V	0	1	0	0	0	1	0	0
2V	0	0	1	0	0	1	0	0
V	0	0	0	1	0	1	0	0
0	1	0	0	0	0	0	0	0
-V	1	0	0	0	0	0	1	0
-2V	0	1	0	0	0	0	1	0
-3V	0	0	1	0	0	0	1	0
-4V	0	0	0	1	0	0	1	0

The Switching sequence are shown as the above Table we will generate the required pulse from the circuit

HPWM TOPOLOGY

The Optimized novel HPWM topology is, the combination of carried and reference with the required the pulse generation [4-6] In suggested topology the generation of pulse to ignite the operation of switching devices, the designed HPWM signals generated to obtain the output voltages. The switching pattern are obtained with the combination of carrier signal and reference signal. The Carrier Signal V_c would be associated with V_{ref} until V_{ref} reaches zero. This results in the producers of essential swapping pattern as shown.

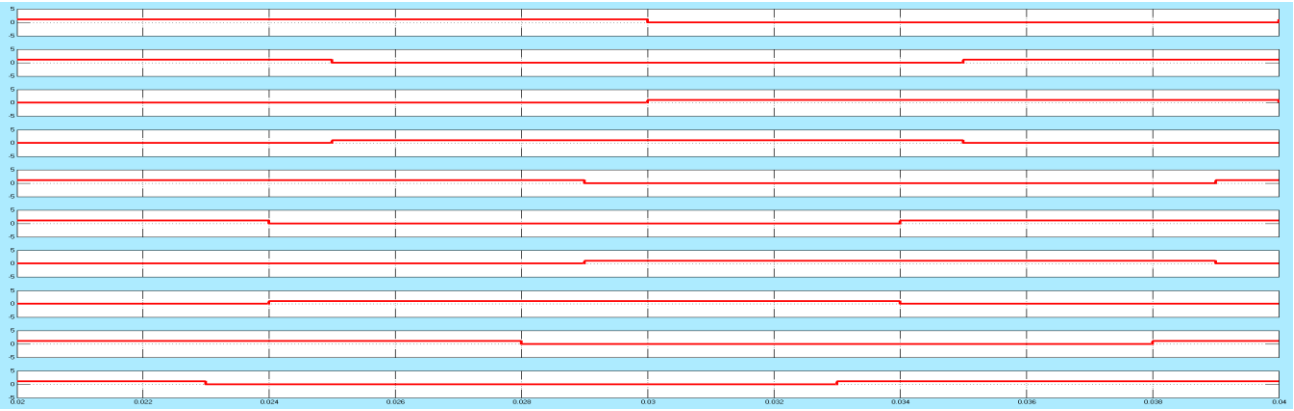

Figure 4.1: Nine level pulse generation

SIMULATION RESULTS

The Optimized novel Nine Level Cascaded Multi-level Inverter operation and the voltage and current waveform of CHMLI are verified and compared the intended value The simulation diagram of Novel Hybrid Cascaded Hi bridge Multi Level Inverter is shown in Figure 51.

The switches are used in novel optimized multi-level inverter and voltage balancing circuits. The MOSFET switches are preferred to use in CMLI circuit, In these switches one of the switch be operated in bidirectional and others be operated in unidirectional and the resistive load is occupied as 100 ohms. The dc source voltage is taken as 100V.

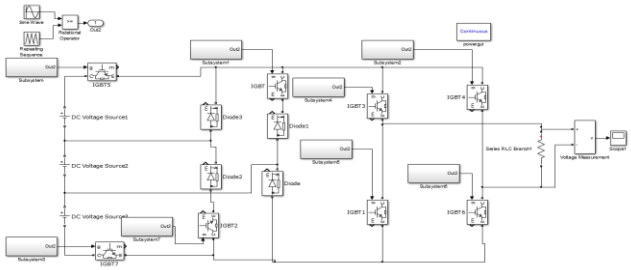

Figure 5.1: iSimulation diagram for nine level multi-level inverter.

The novel CHMLI circuit diagram as shown in the fig5.1 the designed circuit to obtain 11 level output voltage with the reduced no. of switches The Matlab Simulink is executed and verify the yield voltage and current waveform and also THD calculated using FFT analysis.

The Voltage and Current waveform of novel optimize CHMLI as shown in fig5.2 the output voltage waveform in staircase in nature we try to obtain the waveform in smooth sinusoidal waveform The level of output voltages peak to peak voltages is nearly 5V. The Hybrid modulation technique is incorporated in the circuit with the help of HPWM schemes The FFT analysis used to obtain the THD value and verified with calculated once.

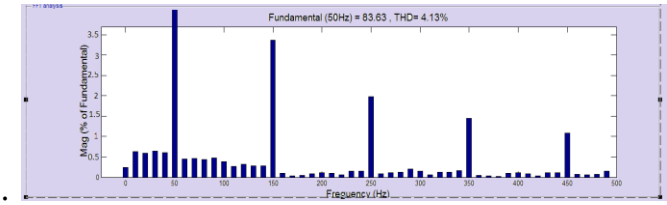

Figure5.2: THD analysis

The suggested novel optimzed HCMLI is executed and calculated the THD value using Fast Fourier Transform (FFT) study is display in figure 5.3. THD is 4.13f% with a base frequency of 50 Hz for its output ivoltage.

2. CONCLUSION

Optimized HCMLI has been designed with pulse generation using Nine level PWM topologies. The bidirectional switches are used to obtain the swapping the polarity of the supply with separated DC sources. The optimized HPWM topology for harmonic ireduction is Simulated using MATLAB/SIMULINK. The THD analysis for the designed CMLI is obtained with fundamental frequency of 50Hz.The suggested methodology is incorporated with the less number of switches with voltage ibalancing circuit. The future scope of the CMLI smoothening the wage form and less THD value for the electric vehicle application

3. REFERENCES

[1] Martha Calais, Lawrence J. Borlel Vassilios, *G.* Agelidis “Analysis of Multicarrier PWM Methods for a Single-phase Five Level Inverter”, IEEE Transactions on Power Electronics, July 2001, pp 1351-1356.

[2] J. Rodr´ıguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002
[3] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec.*2007.
[4] S. Kouro, J. Rebolledo, and J. Rodriguez, "Reduced switching frequency modulation algorithm for high-power multilevel inverters," IEEE Trans.Ind. Electron., vol. 54, no. 5, pp. 2894–2901, Oct. 2007
[5] M.G.H.Aghdam, S.H.Fathi, .B.Gharehpetian, "Analysis of multicarrier PWM methods for asymmetric multilevel inverter" in Proc. 3rd IEEE Conference on Industrial Electronics and Applications, ICIEA'08, June 2008, pp.2057 -2062.
[6] M.Malinowski, K. Gopakumar, J. Rodr´ıguez, andM. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron., vol. 57,* no. 7, pp. 2197–2206, Jul. 2010.
[7] C. Govindaraju and K. Baskaran, "Efficient hybrid carrier based space vector modulation for cascaded multilevel inverter," *J. Power Electron.*, vol. 10, no. 3, pp. 277–284, May 2010.
[8] Satish kumar and Dr M. Sasikumar "An Approach of Hybrid Modulation in Fusion seven-level Cascaded Multilevel Inverter accomplishment to IM drive system"2016 Second International Conference On Science Technology Engineering and Management(ICONSTEM) 978-1-5090-1706-5, 2016 IEEE pp 384-387
[9] N Sujitha, S Satish Kumar, M Sasikumar " Design And Implementation Of Hybrid Spwm Control For Cascaded H-Bridge Multi Level Inverter For Motor Drives, "IU-Journal Of Electrical & Electronics Engineering, vol. 14, no.1, pp. 1721-1727. Impact Factor:- 0.14,March 2014
[10] S.Satish kumar and Dr M. Sasikumar0(2020) "Asymmetric hybrid multilevel inverter with reduced harmonic using hybrid modulation technique " International Journal of Power Electronics and Drive System (IJPEDS) ISSN: 2088-8694, DOI: 10.11591/ijpeds.v11.i2.pp605-610 Volume11 issue2 June 2020 pp no 605-610
[11] S.Satish kumar and Dr M. Sasikumar (2021) "Intelligent hybrid technique for cascaded multilevel inverter based three phase grid‑tie hybrid power system: a WPSNN technique" Journal of Ambient Intelligence and Humanized Computing 1868-513702 Jan 2021.
[12] P.Sivaperumal , S.S.Dash,, K.Mohanraj and C.Balaji,"Switched Coupled Inductor Inverter based Interline Dynamic Voltage Restorer with DWT-ANN Technique", International Journal of Electrical Engineering & Education, 1-18, 2019
[13] P.Sivaperumal , S.S.Dash, and k.Saravanan, "Mitigation of Power Quality Issues Using SMES Based DVR aided Switched Coupled Inductor Inverter", Measurement and Control , 52 (9-10), 1329-1343, 2019.
[14] T. Sasilatha Balaji. S & P. Suresh Mohan Kumar, "Detection of Multi-Layer Attack using Anticipated Relay Algorithm in the Wireless Sensor Networks", Int. J. Mech. Product. Eng. Res. Dev.(IJMPERD), vol.8, s2,2018.
[15] V Karthikeyan, V Jamuna, I William Christopher, "Phase Disposition PWM Based Multi Level Inverter with Reduced Number of Switches", Advanced Aspects of Engineering Research, Vol. 7, pg.1-15,2021.
[16] Zhou Jinghua and Li Zhengxi, ―Research on Hybrid Modulation Strategies Based on General Hybrid Topology of Multilevel Inverter‖, International symposium on Power

Electronics Electrical Drives, Automation & Motion, IEEE Conf. Rec: 978-1-4244-1664-6, pp.784-788, 2008.

[17] P Muthukumar, Padma Suresh Lekshmi Kanthan, T Baldwin Immanuel, K Eswaramoorthy, "FPGA Performance Optimization Plan for High Power Conversion", International Conference on Soft Computing Systems, Springer, 491-502,2018.

[18] Lakshmi, D., Baskaran, S., Ezhilarasi, G., Valli, C., Direct AC/DC power converter using auxiliary circuits, International Journal of Advanced Science and Technology, 2020, 29(7 Special Issue), pp. 785–793

[19] JS Ashwin, N Manoharan "Power of Ambient Temperature on the Performance of the Semiconductor Laser" IJEECS, ISSN:2502-4752, Vol. 9, No. 3, March 2018, pp. 606~608.

[20] V Mythili, A Suresh, Merlin M Devasagayam, R Dhanasekaran SEAT-DSR: Spatial and energy aware trusted dynamic distance source routing algorithm for secure data communications in wireless sensor networks Cognitive Systems Research 58 143-155 Elsevier

[21] G Jegadeeswari, (2019)"Performance Analysis of Power Quality Improvement using Shunt Active Power Filter" International Journal of Recent Technology and Engineering (IJRTE), 7 (5), 1-3

[22] M Parameswari, T Sasilatha, (2018)"Cross-layer based error control technique for WSN with modified relay node selection and corruption aware method" Wireless Personal Communications 99 (1), 479-495

[23] A Priya, T Sasilatha (2017) "Wireless network for strategic boundary supervision system" Bulletin of Electrical Engineering and Informatics 6 (4), 367-370